Canny Edge Detector

Final Demonstration

Team Members:

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# Agenda

1. Synthesize entire design and show that synthesis does not generate any inferred latches, timing arcs, or sensitivity list warnings
2. Show previously generated IC layout and demonstrate that all geometry and connectivity checks are passed
3. Show chip area, I/O pin count, throughput, and clock rate values
4. Run test bench 1 in source (interfacing with SRAM)
5. Run test bench 2 in source (generating image after Gaussian blur)
6. Run test bench 3 in source (generating image after magnitude calculations)
7. Run test bench 4 in source (generating image after non-maximum suppression)
8. Run test bench 5 in source (generating final output image)
9. Show waveforms from test bench 5 in source match waveforms from previously run test bench 5 in mapped

# Fixed Success Criteria

1. (2 pts) Test benches exist for all top-level components and the entire design. The test benches for the entire design can be demonstrated or documented to cover all of the functional requirements given in the design specific success criteria.

* Status:
* Agenda Item(s): 4, 5, 6, 7, 8, 9

1. (4 pts) Entire design synthesizes completely, without any inferred latches, timing arcs, and, sensitivity list warnings.

* Status:
* Agenda Item(s): 1

1. (2 pts) Source and mapped version of the complete design behave the same for all test cases. The mapped version simulates without timing errors except at time zero.

* Status:
* Agenda Item(s): 9

1. (2 pts) A complete IC layout is produced that passes all geometry and connectivity checks.

* Status:
* Agenda Item(s): 2

1. (2 pts) The entire design complies with targets for area, pin count, throughput (if applicable), and clock rate. The final targets for these parameters will be determined by course staff based on your design review. Failure to reach any of the targets will result a score of 1 out of 2 provided that you are within 50% on area, 10% on pin count, and 25% on throughput. Doing worse in any category will result in a score of 0 out of 2.

* Status:
* Demonsration(s): 3

**Design Specific Success Criteria**

1. (1 pt) Demonstrate by simulation of a Verilog test bench that the design can successfully interface with the off-chip SRAM module (both read and write capabilities).

* Status:
* Agenda Item(s): 4

1. (1 pt) Demonstrate by simulation of a Verilog test bench that Gaussian block of the design performs the correct Gaussian convolution algorithm on the original image pixel data.

* Status:
* Agenda Item(s): 5

1. (1 pt) Demonstrate by simulation of a Verilog test bench that the Gradient/Magnitude block of the design performs the correct gradient convolution algorithm and calculates the correct magnitudes based on the data provided by the Gaussian block.

* Status:
* Agenda Item(s): 6

1. (1 pt) Demonstrate by simulation of a Verilog test bench that the Suppression block of the design correctly calculates pixel angles, compares the angles of neighboring pixels, passes out the appropriate values based on the data provided by the Gradient/Magnitude block.

* Status:
* Agenda Item(s): 7

1. (1 pt) Demonstrate by simulation of a Verilog test bench that the Hysteresis block is able to accurately determine if pixels are/are not part of en edge using the defined thresholds and based on the data provided by the Suppression block.

* Status:
* Agenda Item(s): 8

1. (3 pts) Demonstrate by simulation of a Verilog test bench that the complete design is able to produce an output bitmap image with the edges in the original image accurately detected.

* Status:
* Agenda Item(s): 8, 9